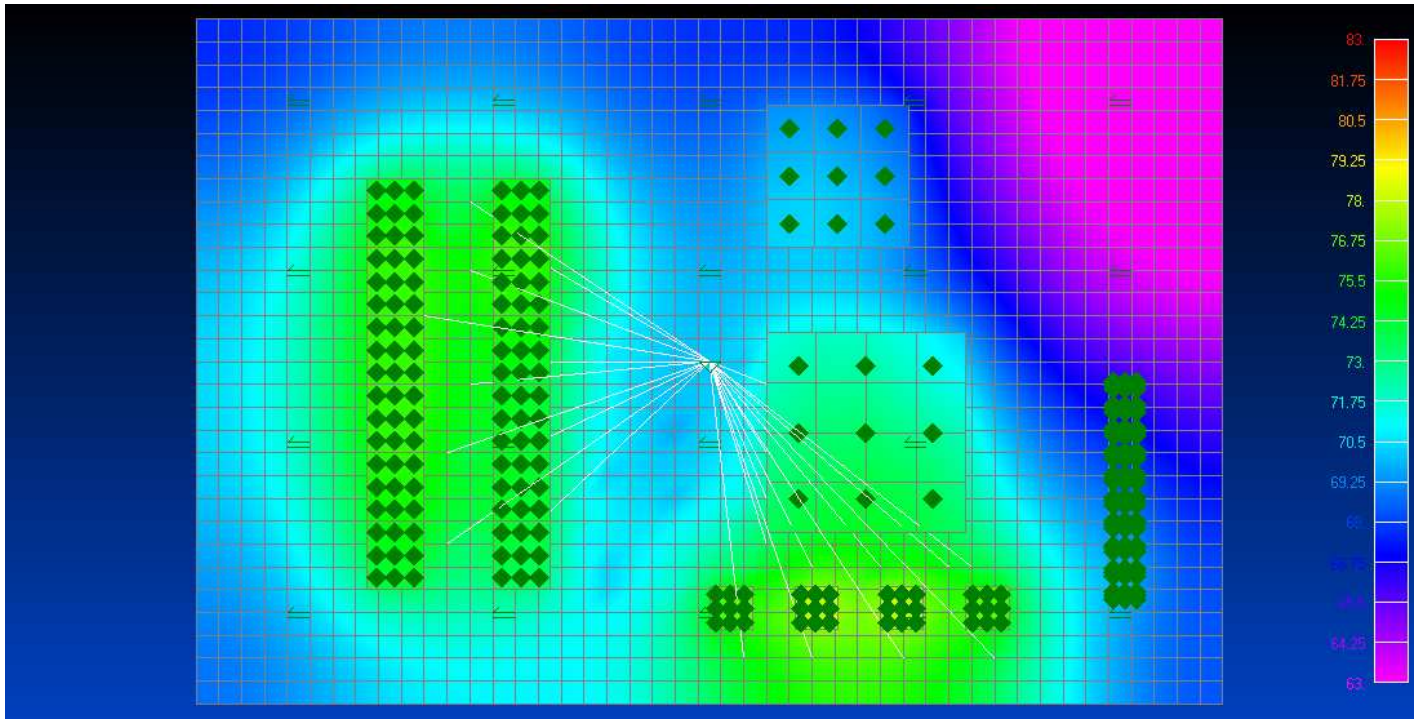
Thermal Vias Design Optimization



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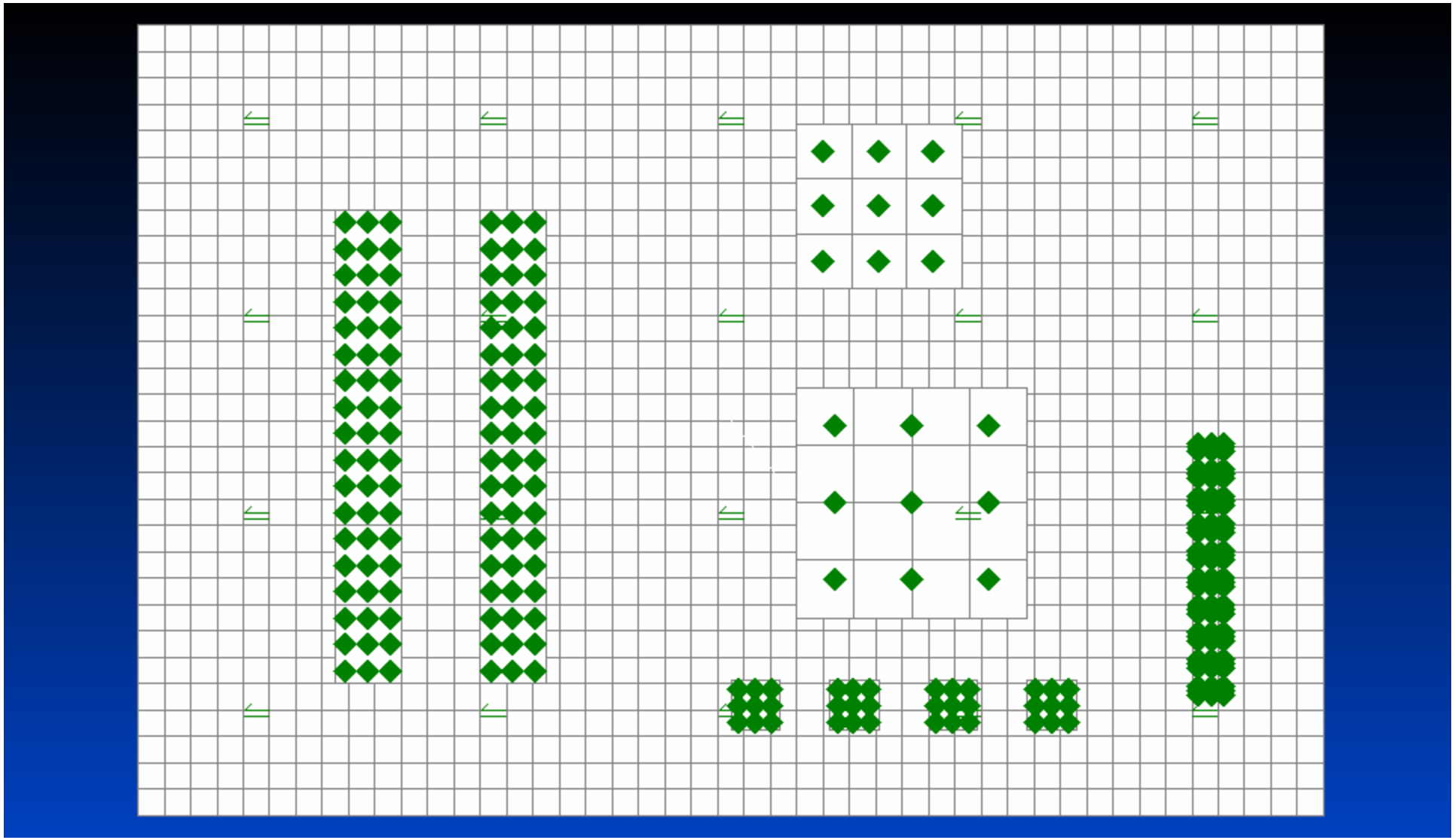
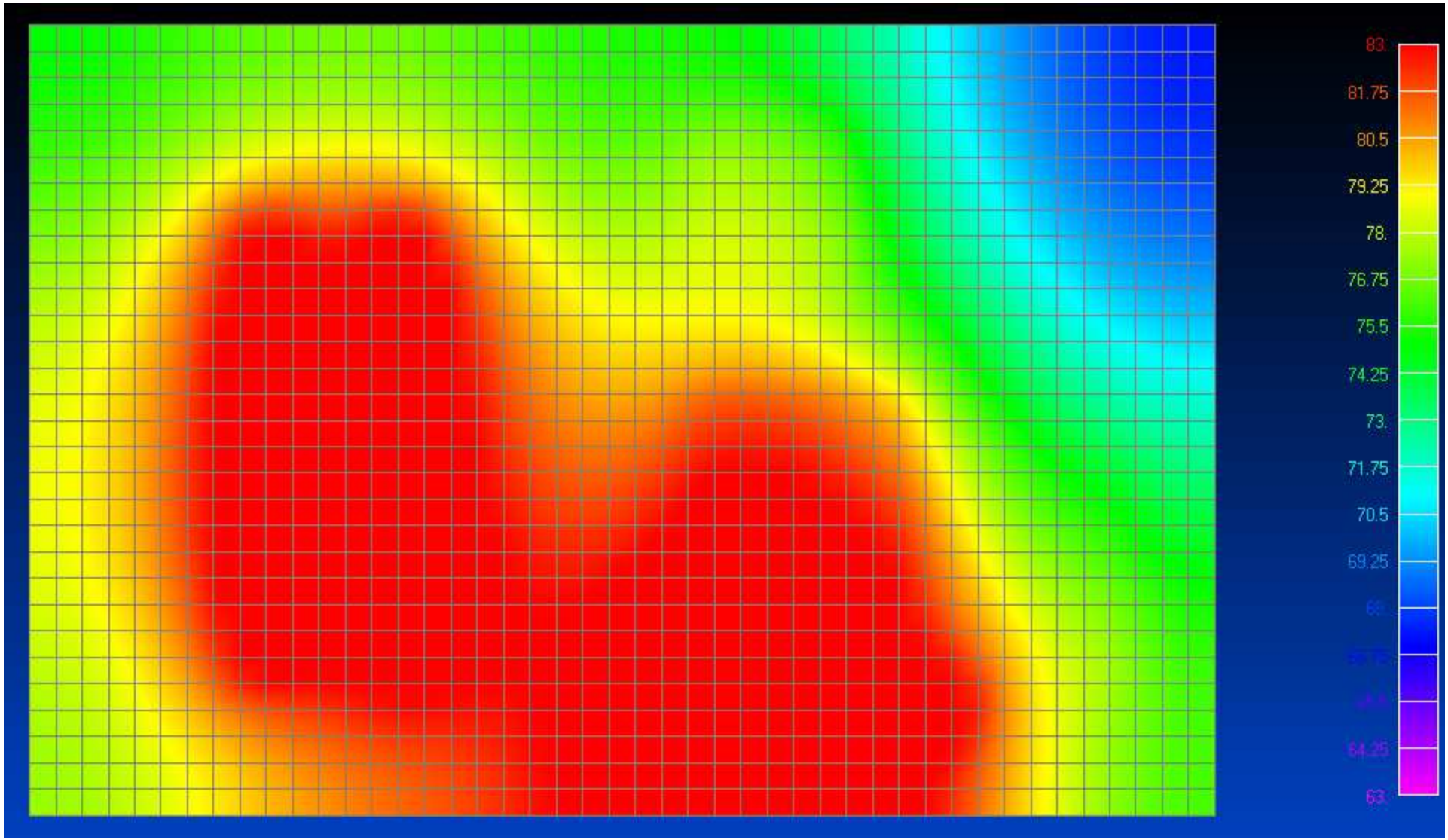
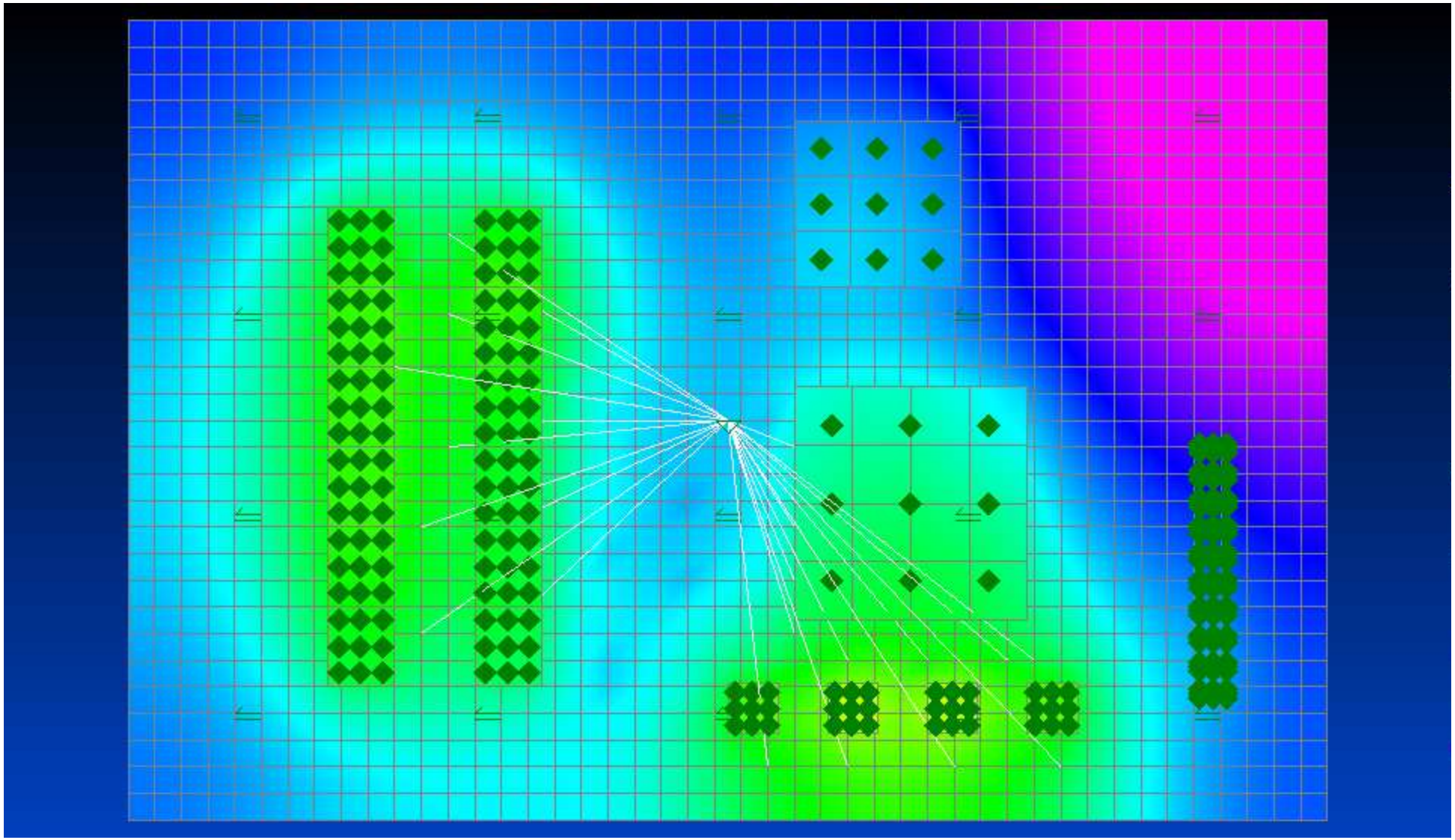
Electronics Board with Heat Loads on Device Footprints



Board temperatures without vias. Convective cooling only.



Find optimum configuration of 5 thermal vias out of 22 possible via sites in order to minimize the maximum board temperature. Vias are connected to 25 ºC plane. (Via sites shown as white line elements below.)



To find the optimum configuration run the model with all possible configurations.

- There are 22,634 configurations to consider.

$$N = \frac{p!}{(p-q)!q!}$$

- Vias are 0.254 mm diameter holes plated with copper thickness of 0.05mm and 3mm long.
- Vias are modeled as link elements connected to a boundary node at T=25^{o}C.

This is easy accomplish with some simple code in *SINDA/G.*

With a 3.2 GHertz machine this takes about 9 minutes to run all 22,634 cases.

```
      BCD 3EXECUTION
F     kk=1        !kk is run #
F     n=22        !n is number of total number of vias in config space
F     do i1=1,n
F     do i2=i1+1,n
F     do i3=i2+1,n
F     do i4=i3+1,n
F     do i5=i4+1,n
F     G(5736:5757)=0.0              ! Zero link elements
F     G(i1+5735)=0.1650000E-02 ! Load link elements
F     G(i2+5735)=0.1650000E-02
F     G(i3+5735)=0.1650000E-02
F     G(i4+5735)=0.1650000E-02
F     G(i5+5735)=0.1650000E-02
      SNSOR
F     DATA(kk,1)=i1
F     DATA(kk,2)=i2
F     DATA(kk,3)=i3
F     DATA(kk,4)=i4
F     DATA(kk,5)=i5
F     DATA(kk,6)=MAXVAL( T(NR(10001):NR(11426)) )
F     enddo
F     enddo
F     enddo
F     enddo
F     enddo
```

The best configuration lowered maximum board T 5ºC.